Docket No. 200314997-1

Amendments to the Claims:

Status of Claims:

Claims 1-24 are pending for examination.

Claim 1, 9, 10, 11, and 12 are amended herein.

Claims 1, 11, 14, 22, 23, and 24 are in independent form.

1. (Currently Amended) A system for simulating a processor performance state in a processor, comprising:

a data structure stored in a memory, the data structure being configured to store an address of a GPIO (general purpose input output) block and a set of bit patterns that may be written to one or more of, the GPIO block and a thermal management register in the processor, where the GPIO block is configured to control a thermal management signal that can be provided to the processor, and

a logic operably connected to the memory, the logic configured to receive a request to establish a desired processor performance state in the processor, to select a bit pattern ~~to be written to the GPIO block or the thermal management register~~, the bit pattern being selected from the set of bit patterns, and to write the bit pattern to the GPIO block or the thermal management register, where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state.

2. (Original) The system of claim 1, where the data structure is further configured to store an address of an ACPI status register from which a value related to a frequency and a voltage established in the processor can be read.

3. (Original) The system of claim 1, where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function.

4. (Original) The system of claim 1, where the data structure comprises an ACPI table stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling a processor function.

5. (Original) The system of claim 1, where the data structure comprises an ACPI table stored in a Basic Input Output System (BIOS) configured to facilitate controlling a processor function.

6. (Original) The system of claim 1, where the set of bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state.

7. (Original) The system of claim 1, where the thermal management register comprises the TM2 register in a Pentium microprocessor.

8. (Original) The system of claim 1, where the thermal management signal comprises a signal placed on the PROCHOT line available to a Pentium microprocessor.

9. (Currently Amended) The system of claim 1, the system being incorporated into a computer.

~~A computer configured with a system for simulating a processor performance state in a processor, the system comprising:~~

~~a data structure stored in a memory, the data structure being configured to store an address of a GPIO block and a set of bit patterns that~~

~~may be written to one or more of, the GPIO block and a thermal management register in the processor, where the GPIO block is configured to control a thermal management signal that can be provided to the processor, and~~

~~a logic operably connected to the memory, the logic configured to receive a request to establish a desired processor performance state in the processor, to select a bit pattern to be written to the GPIO block or the thermal management register, the bit pattern being selected from the set of bit patterns, and to write the bit pattern to the GPIO block or the thermal management register, where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state.~~

10. (Currently Amended) The system of claim 1, the system being incorporated into a printer.

~~A printer configured with a system for simulating a processor performance state in a processor, the system comprising:~~

~~a data structure stored in a memory, the data structure being configured to store an address of a GPIO block and a set of bit patterns that may be written to one or more of, the GPIO block and a thermal management register in the processor, where the GPIO block is configured to control a thermal management signal that can be provided to the processor, and~~

~~a logic operably connected to the memory, the logic configured to receive a request to establish a desired processor performance state in the processor, to select a bit pattern to be written to the GPIO block or the thermal management register, the bit pattern being selected from the set of bit patterns, and to write the bit pattern to the GPIO block or the thermal management register, where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state.~~

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11. (Currently Amended) A system for simulating a processor performance state in a processor that is configured to receive an actual thermal management signal from a thermal management circuit and to selectively change the processor ~~its~~ operating frequency based on the actual thermal management signal, the system comprising:

a simulation logic configured to produce a simulated thermal management signal; and

a combination logic configured to selectively provide to the processor one and only one of, the actual thermal management signal and the simulated thermal management signal.

12. (Currently Amended) The system of claim 11, where the simulation logic comprises:

a data structure stored in a memory, the data structure being configured to store an address of a GPIO block and a set of bit patterns that may be written to one or more of, the GPIO block and a thermal management register in the processor, where the GPIO block is configured to control a thermal management signal that can be provided to the processor, and

a logic operably connected to the memory, the logic configured to receive a request to establish a desired processor performance state in the processor, to select a bit pattern ~~to be written to the GPIO block or the thermal management register~~, the bit pattern being selected from the set of bit patterns, and to write the bit pattern to the GPIO block or the thermal management register, where the bit pattern facilitates controlling a frequency and a voltage at which the processor will operate, thus simulating the desired processor performance state.

13. (Original) The system of claim 11, where the processor is a Pentium 4 microprocessor.

14. (Original) A method for simulating a processor performance state, comprising:

receiving a request to establish a processor performance state in a processor;

accessing a data store to acquire simulation data that facilitates controlling the state of a thermal management signal and a thermal management register; and

causing the processor performance state to be simulated by causing the processor to change its operating frequency and operating voltage in response to a thermal management signal produced in response to writing a bit pattern to a GPIO block.

15. (Original) The method of claim 14, including establishing a data structure as an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor.

16. (Original) The method of claim 15, where establishing the data structure includes writing a set of bit patterns to the ACPI table and writing the address of the GPIO block to the ACPI table.

17. (Original) The method of claim 14, where the processor performance state corresponds to one of, a higher performance state, and a lower performance state.

18. (Original) The method of claim 14, where the simulation data comprises a set of bit patterns that can be written to one or more of, the thermal management register, and the GPIO block.

19. (Original) The method of claim 14, where the thermal management register comprises the TM2 register in a Pentium microprocessor.

20. (Original) The method of claim 14, where the thermal management signal comprises the PROCHOT signal available to a Pentium microprocessor.

21. (Original) The method of claim 14, including:

acquiring an address of an ACPI status register configured to report a value related to the operating frequency and the operating voltage of the processor;

reading the value from the ACPI status register; and

selectively reporting a success or error condition based on the value.

22. (Original) A computer-readable medium storing processor executable instructions operable to perform a method for simulating a processor performance state in a processor, the method comprising:

receiving a request to establish a processor performance state in a processor;

accessing a data store to acquire simulation data that facilitates controlling the state of a thermal management signal and a thermal management register; and

causing the processor performance state to be simulated by causing the processor to set its operating frequency and operating voltage in response to a thermal management signal produced in response to writing a bit pattern to a GPIO block.

23. (Original) A system, comprising:

means for accessing addresses and bit patterns that facilitate controlling a thermal management signal available to a processor, where the processor is configured to selectively establish its operating frequency and operating voltage based, at least in part, on the thermal management signal;

means for receiving a request to place the processor into a processor performance state; and

means for simulating a processor performance state by writing a bit pattern to a logic configured to control the thermal management signal.

24. (Original) A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a processor performance state in a processor by controlling a thermal management signal, comprising:

a first interface for communicating a bit pattern data;

a second interface for communicating a GPIO block address data; and

a third interface for communicating a state data, where the state data is related to a simulated processor performance state generated by applying the bit pattern data to a GPIO block identified by the GPIO block address data.